CLAIMS

1. A method of programming a multi-level, electrically-programmable memory including memory cells electrically programmable into at least two distinct programmed states, the method comprising:

defining at least two programming sequences, each programming sequence being designed for electrically programming memory cells into at least one respective programmed state;

selecting a group of memory cells of the memory;

receiving a pattern of data to be written into the selected group of memory cells of the memory;

analysing the pattern for determining sub-groups of memory cells, each sub-group of memory cells including the memory cells in the selected group that are to be brought into at least one respective programmed state of the at least two distinct programmed states; and

submitting the memory cells in each sub-group to the respective programming sequence.

2. The method of claim 1, including submitting the different sub-groups of memory cells to the respective programming sequences in succession.

3. The method of claim 2, wherein the submitting in succession includes establishing a memory cell sub-group programming succession such that biasing conditions in which the memory cells of any given sub-group are verified as programmed to the desired programmed state are substantially close to biasing conditions in which the memory cells will be read in a standard read access.

4. The method of claim 3, wherein the establishing the memory cell sub-group programming succession includes ordering the sub-group of memory cells according to a decreasing distance of the corresponding programming states from a non-programmed state of the memory cells.

5. The method of claim 1, wherein each of the at least two programming sequences includes applying to a control electrode of the memory cells a voltage ramp, the at least two programming sequences having voltage ramps of different slope.

6. The method of claim 5, including submitting the different sub-groups of memory cells to the respective programming sequences in succession.

7. The method of claim 6, wherein the submitting in succession includes establishing a memory cell sub-group programming succession such that biasing conditions in which the memory cells of any given sub-group are verified as programmed to the desired programmed state are substantially close to biasing conditions in which the memory cells will be read in a standard read access.

8. The method of claim 7, wherein the establishing the memory cell sub-group programming succession includes ordering the sub-group of memory cells according to a decreasing distance of the corresponding programming states from a non-programmed state of the memory cells.

9. The method of claim 5, wherein a programming sequence associated with a programmed state closest to a non-programmed state of the memory cells includes applying to the control electrode of the memory cells a voltage ramp having a first slope.

10. The method of claim 9, wherein at least one of the programming sequences associated with programmed states intermediate between the state closest to and the state most distant from the non-programmed state includes:

applying to a control electrode of the memory cells a first voltage ramp having a third slope intermediate between the first slope and the second slope;

verifying the programmed state of the memory cells;

as soon as one of the memory cells is verified to have reached the desired programmed state, applying to the control electrode of the memory cells a second voltage ramp having a fourth slope equal to or higher than the first slope, but lower than the third slope.

11. The method of claim 9, wherein a programming sequence associated with a programmed state most distant from the non-programmed state of the memory cells includes applying to a control electrode of the memory cells a voltage ramp having a second slope higher than the first slope.

12. The method of claim 11, wherein at least one of the programming sequences associated with programmed states intermediate between the state closest to and the state most distant from the non-programmed state includes:

applying to a control electrode of the memory cells a first voltage ramp having a third slope intermediate between the first slope and the second slope;

verifying the programmed state of the memory cells;

as soon as one of the memory cells is verified to have reached the desired programmed state, applying to the control electrode of the memory cells a second voltage ramp having a fourth slope equal to or higher than the first slope, but lower than the third slope.

13. The method of claim 11, including submitting the different sub-groups of memory cells to the respective programming sequences in succession.

14. The method of claim 13, wherein the submitting in succession includes establishing a memory cell sub-group programming succession such that biasing conditions in which the memory cells of any given sub-group are verified as programmed to the desired programmed state are substantially close to biasing conditions in which the memory cells will be read in a standard read access.

15. The method of claim 14, wherein the establishing the memory cell sub-group programming succession includes ordering the sub-group of memory cells according to a decreasing distance of the corresponding programming states from a non-programmed state of the memory cells.

16. The method of claim 1, including:

defining a default programming sequence, the default programming sequence being designed so as to be adapted to bring a memory cell into any one of the programmed states;

defining an average programming time required on average for programming the selected group of memory cells using the default programming sequence;

after having determined the sub-groups of memory cells, estimating an overall programming time required for programming the selected group of memory cells using the at least two programming sequences;

comparing the estimated overall programming time to the average programming time; and

if the estimated overall programming time exceeds the average programming time, programming the selected group of memory cells using the default programming sequence.

17. The method of claim 16, wherein the default programming sequence corresponds to a programming sequence associated with a programmed state closest to the non-programmed state of the memory cells.

18. A multi-level, electrically-programmable memory with memory cells electrically programmable into at least two distinct programmed states, comprising:

means for determining sub-groups of memory cells within a selected group of memory cells to be electrically programmed, each sub-group of memory cells including the memory cells in the selected group that are to be brought into at least one respective programmed state of the at least two distinct programmed states; and

means for submitting the memory cells in each sub-group to a respective programming sequence.

19. A computing system comprising:

a computing circuit; and

at least one memory circuit, electrically coupled with the computing circuit, each of the at least one memory circuit including :

a multi-level, electrically-programmable memory with memory cells electrically programmable into at least two distinct programmed states, comprising:

means for determining sub-groups of memory cells within a selected group of memory cells to be electrically programmed, each sub-group of memory cells including the memory cells in the selected group that are to be brought into at least one respective programmed state of the at least two distinct programmed states; and

means for submitting the memory cells in each sub-group to a respective programming sequence.